## ***REMARKS***

### *Summary of the Amendment*

Upon entry of the present Amendment, Claims 25, 35 and 44 will have been amended. Accordingly, Claims 25-44 remain pending in the present application.

### *Summary of the Official Office Action*

In the subject Office Action, the Drawings, Abstract and Claims 25 and 44 have been objected to by the Examiner over matters pertaining to form. Moreover, Claims 25-44 have been rejected over the art of record. By the present Amendment and Remarks, Applicant submits that the rejections have been overcome, and respect requests reconsideration of the Office Action and an allowance of the present application.

### *Informal Telephone Interview with Examiner Nhu*

Applicant appreciates the courtesy extended to their representative by Examiner Nhu in an informal telephone interview conducted on May 19th, 2004. In the interview Applicant pointed out distinguishing features of the present invention as well as deficiencies of the art of record. In particular, Applicant's representative pointed out to Examiner Nhu that Lo et al. (U.S. Patent 6,507,120) does not teach or even suggest a lead 20 having first and second opposing surface 21, 22 *and a third surface 23 disposed between the first and second surfaces 21, 22*, as is taught by the Applicant's invention. The Examiner acknowledged that Lo et al. did not teach a third surface as taught by the present invention, and agreed to further consider Applicant's arguments, in light of the interview, when submitted in a formal response.

### *Traversal of Objection to Drawings*

Applicant traverses the objection to Figure 4 in which the Examiner suggests that Figure 4 does not properly reference a conductive layer 24. Figures 1, 1B-D, 2, 2B-2D, 3 and 3B-D depict a conductive layer 24. However, the embodiment shown in Figure 4 does not include the conductive layer 24. As stated in paragraph **[0019]**, "[r]eferring now to Figure 4, *as an alternative to the conductive layer 24, each of the leads 20 may be provided*

*with a protective layer 24a on the third surface 23 thereof*". Therefore, Figure 4 as submitted properly references protective layer 24a which replaces the conductive layer 24.

Furthermore, Applicant has submitted a "Replacement Sheet" (see attached) for Figure 4 which adds a reference numeral "23" to indicate the third planar surface which is similar to Figures 1, 1B-D, 2, 2B-2D, 3 and 3B-D.

Accordingly, Applicant submits that the objection to Figure 4 has been overcome, and further requests that the Examiner indicate approval of the attached "Replacement Sheet" for Figure 4 in the next Office Action.

***Objection to Abstract***

The Abstract has been objected to because legal phraseology such as "comprise" was included therein. The Applicant has amended the Abstract and, in particular, has eliminated usage of the word "comprise". Accordingly, Applicant requests that the Examiner withdraw the objection to the Abstract.

***Objection to the Claims***

The Examiner has objected to the form of Claims 25 and 44 by suggesting that the phrase "the third surfaces" should be -- the third surface -- . Applicant has made the suggested amendment to expedite prosecution. Accordingly, Applicant requests that the Examiner reconsider and withdraw the objection to the form of the claims.

***Traversal of Rejection Under 35 U.S.C. § 103(a)***

Applicant respectfully traverses the rejection of Claims 25-44 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,507,120 B2 to Lo et al. [hereinafter "LO"] in view of U.S. Patent No. 6,208,021 B1 to Ohuchi et al. [hereinafter "OHUCHI"].

*A Review of LO*

LO discloses a flip chip quad flat non-lead package comprising a plurality of leads 202 each having a first surface 204 and second surface 206; a die 210 having an active surface 212 and a backside 214 opposite to the active surface 212, wherein the active surface 212 has a plurality of bonding pads 216, each having a bump 218, and wherein each bump

218 is connected to the first surface 204 of a respective one of the leads 202; and a molding compound 224 encapsulating the leads 202 and the die 210, exposing the second surfaces 206 of the leads 202. It is preferred that the first surfaces 204 of leads 202 are each covered by a solder mask 220. Figure 5 depicts a locally enlarged perspective view of leads 202 in Figure 2. Preferably, a solder resistance process is carried out to form the solder mask 220 on the first surface 204 of each of the leads 202. The solder mask 220 defines an opening 222 to accommodate on of the bumps 218.

*A Review of OHUCHI*

OHUCHI discloses a high density resin sealing type semiconductor device having spot leads 7 adhered to a circuit forming surface of a semiconductor element 1 via an insulative adhesive tape 2 interposed therebetween. The spot leads 7 are partially coated with metal plating 8 for an external terminal (an upper surface side in Figure 3) and for an internal connection (a lower surface side in Figure 3).

*The Present Invention*

Applicant's independent Claims 25, 35 and 44, as amended recite, *inter alia*, . . . a plurality of ***homogenously*** formed leads which each include a first surface, a second surface disposed in opposed relation to the first surface, ***and a third surface disposed in opposed relation to the second surface and oriented between the first and second surfaces***; . . . In *Webster's* Ninth New Collegiate Dictionary, the word "homogeneous" is defined as "of uniform structure or composition throughout".

Moreover, Applicant's independent Claims 25, 35 and 44 further recite, *inter alia*, . . . applying encapsulant to the leads . . . . such that ***the first and a portion of the third surface of each of the leads are covered by the encapsulating portion*** . . . .

*LO Does Not Teach or Suggest a Lead With Three Surfaces*

As stated *supra*, LO teaches a plurality of leads 202 each having a first surface 204 and second surface 206. However, it is clearly evident that LO does not teach, *inter alia*, a plurality of ***homogenously*** formed leads which each include a first surface, a second

surface disposed in opposed relation to the first surface, ***and a third surface disposed in opposed relation to the second surface and oriented between the first and second surfaces***; . . .

Initially, it is not clear as to which features of LO the Examiner considers to be the first, second and third surfaces of the leads. It appears that the Examiner has interpreted the upper surface of the LO solder mask 220 to be the first surface, the lower surface 206 of the LO lead 202 to be the second surface, and the upper surface 204 of the LO lead 202 to be the third surface. *This interpretation is inappropriate, and in reality, one of ordinary skill in the art would properly interpret the LO leads 202 as having only an upper surface 204 and lower surface 206.* Even if the interpretation provided by the Examiner is appropriate (which Applicant does not submit), LO still does not teach or suggest, *inter alia*, . . . a plurality of ***homogenously*** formed leads . . . as is now recited in amended Claims 25, 35 and 44. Instead, the LO lead 202 as interpreted by the Examiner includes the actual lead 202 and the solder mask 220 *which by definition is not part of a homogeneously formed lead.*

*Neither LO nor OHUCHI Teach or Suggest Covering Both the First and a Portion of the Third Surface of Each of the Leads With the Encapsulating Portion*

It is also evident that the Examiner's argument is further flawed with respect to independent Claims 25, 35 and 44 because the first and portions of the third surface of each of the leads which LO and OHUCHI teach are not capable of being covered by encapsulant.

For instance, the third surface 204 of LO is never exposed to encapsulant 224. Instead, the third surface 204 of LO is covered by either solder mask 220 or by the solder ball 218. Similarly, assuming that the third surface of OHUCHI is defined by a portion of the lead 7 which is covered by either the plating 8 or the adhesive tape 2 (which must necessarily be the case), such third surface is therefore not covered by encapsulant. The same hold true for any surface of the lead 7 in OHUCHI which could be construed as the first surface, since any such surface is also covered by either the plating 8 or adhesive tape 2. Hence, in both LO and OHUCHI, is impossible to apply encapsulant to the first and a

portion of the third surface of each of the leads, as recited in independent Claims 25, 35 and 44. Therefore, based on the foregoing, LO does not teach or suggest a homogeneously formed lead defining the first, second, and third surfaces recited in Claims 25, 33, and 44, with neither LO nor OHUCHI teaching or suggesting, when considered individually or in combination, *inter alia*, . . . *applying encapsulant to the leads . . . . such that* ***the first and a portion of the third surface of each of the leads are covered by the encapsulating portion*** . . . . as recited in Claims 25, 33 and 44.

Accordingly, Applicant respectively requests the Examiner to reconsider and withdraw the rejection of Claims 25, 35 and 44 under 35 U.S.C. § 103(a) and indicate that these claims are allowable over the art of record.

*Dependent Claims 26-34 and 36-43 Are Allowable*

Further, for the foregoing reasons, Applicant submits that Claims 26-34 and 36-43 are allowable at least for the reason that these claims depend from allowable base claims and because these claims recite additional features that further define the present invention.

In particular, Applicant submits that no proper combination of LO and OHUCHI discloses or suggests, *inter alia*, wherein step (a) comprises: 1) providing a wafer having a plurality of semiconductor dies connected to each other via scribing lines; and 2) separating semiconductor dies from the wafer by sawing the wafer along the scribing lines, as recited in Claim 26; wherein step (1) further comprises fusing the conductive bumps to the bond pads of each of the semiconductor dies of the wafer, as recited in Claim 27; wherein step (a) comprises fusing the conductive bumps to respective ones of the bond pads of the semiconductor die, as recited in Claim 28; wherein: step (b) comprises plating a conductive layer onto the third surface of each of the leads; and step (c) comprises electrically and mechanically connecting the conductive bumps to respective ones of the conductive layers, as recited in Claim 29; wherein step (b) comprises providing a die paddle having opposed first and second surfaces and a peripheral edge, and positioning the leads about the peripheral edge of the die paddle in spaced relation thereto, as recited in Claim 30; wherein step (c) comprises bonding the second surface of the semiconductor die to the first surface of the die paddle, as recited in Claim 31; wherein step (d) comprises forming the

encapsulating portion such that the second surface of the die paddle is exposed therein, as recited in Claim 32; wherein step (d) comprises forming the encapsulating portion such that the first surface of the semiconductor die is exposed therein, as recited in Claim 33; wherein step (d) comprises forming the encapsulating portion such that the first surface of the semiconductor die is exposed therein, as recited in Claim 34; wherein step (c) comprises forming the protective layer through an electroplating technique, as recited in Claim 36; wherein step (c) comprises forming the protective layer through an electroless plating technique, as recited in Claim 37; wherein step (b) comprises providing a die paddle having opposed first and second surfaces and a peripheral edge, and positioning the leads about the peripheral edge of the die paddle in spaced relation thereto, as recited in Claim 38; wherein step (d) comprises bonding the second surface of the semiconductor die to the first surface of the die paddle, as recited in Claim 39; wherein step (e) comprises forming the encapsulating portion such that the second surface of the die paddle is exposed therein, as recited in Claim 40; wherein step (e) comprises forming the encapsulating portion such that the first surface of the semiconductor die is exposed therein, as recited in Claim 41; wherein step (e) comprises forming the encapsulating portion such that the first surface of the semiconductor die is exposed therein, as recited in Claim 42; and wherein step (e) comprises forming the encapsulating portion such that at least a portion of each of the leads is exposed therein, as recited in Claim 43.

Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of the aforementioned dependent claims under 35 U.S.C. § 103(a) and indicate that these claims are allowable over the art of record.

Therefore, Applicant respectfully submits that each and every pending claim of the present application meets the requirements for patentability under 35 U.S.C. § 103(a), and respectfully requests that the Examiner indicate the allowance thereof.

## ***CONCLUSION***

Applicant has discussed the rejections asserted against Claims 25-44 and has shown the rejections to be inappropriate. Furthermore, Applicant has discussed the disclosure of the present application and the recitation of allowable subject matter in the pending claims. Applicant has further discussed the disclosure of the references and the deficiencies thereof. Accordingly, Applicant has provided a clear evidentiary basis supporting the patentability of all the claims in the present application, and respectfully requests an indication to such effect in due course.

Should there be any questions, the Examiner is invited to contact the undersigned at the below listed number.

If any additional fee is required, please charge Deposit Account Number 19-4330.

Respectfully submitted,

Date: 6/8/04 By: _____

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